What is claimed is:

1. A semiconductor memory device, comprising:

a cell region;

a peripheral circuit region adjacent to the cell region; and

a plurality of line patterns formed in the cell region and the peripheral circuit region, wherein a spacing distance between the line patterns is at least onefold greater than a width of the line pattern.

2. The semiconductor memory device as recited in claim 1, wherein a ratio of the width of the line pattern to the spacing distance between the line patterns in the cell region is about 1:1.

3. The semiconductor memory device as recited in claim 1, wherein a ratio of the width of the line pattern in the cell region to that of the line pattern in the peripheral circuit region is in a range of about 1:1 to about 1:1.3.

4. The semiconductor memory device as recited in claim 1, wherein the line pattern in the peripheral circuit region has a ratio of the width to the spacing distance in a range of about 1:1.05 to about 1:1.30.

5. The semiconductor memory device as recited in claim

1, wherein the line pattern is a conductive pattern.

6. The semiconductor memory device as recited in claim 5, wherein the line pattern is a bit line pattern.

7. A method for fabricating a semiconductor memory device including a cell region and a peripheral circuit region, the method comprising the steps of:

forming a plurality of line patterns in the cell region and the peripheral circuit region, each being formed by stacking a conductive layer and an insulating hard mask;

removing the insulating hard mask formed in the peripheral circuit region;

forming a conductive spacer at sidewalls of each line pattern in the peripheral circuit region, wherein a spacing distance between the line patterns is at least onefold greater than a width of the line pattern;

forming an insulation layer on an entire surface of the resulting structure;

forming a photoresist pattern for forming a contact hole exposing the conductive layer on the insulation layer; and

forming a deep contact hole exposing the conductive layer by etching the insulation layer with use of the photoresist pattern as an etch mask.

8. The method as recited in claim 7, wherein the line pattern in the peripheral circuit region has a ratio of a

width to a spacing distance in a range of about 1:1.05 to about 1:1.30.

9. The method as recited in claim 7, wherein a ratio of a width of the line pattern to a spacing distance between line patterns in the cell region is about 1:1.

10. The method as recited in claim 6, wherein a ratio of the width of the line pattern in the cell region to that of the line pattern in the peripheral circuit region is in a range of about 1:1 to about 1:1.3.

11. The method as recited in claim 6, wherein the conductive spacer is made of any material selected from a group consisting of TiN, TaN, W or WN.